

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) An RGB control circuit for use in television/video display control, comprising:

a display driver current sensor;

a counter circuit and analog output circuit coupled to control the display driver current;

a speeding comparator having a plurality of sets of comparator circuits coupled in parallel with the display driver current sensor as input, for determining and outputting a measure of the difference between the sensed display driver current and a predetermined value thereof; and

a speeding logic circuit having an input coupled to an output of the speeding comparator and further having an output coupled to an input of the counter circuit, and arranged to control the up/down-counting rate of the counter circuit according to said measure of difference in display driver current to provide a variable up counting rate and a variable down counting rate.

2. (Previously Presented) The RGB control circuit of claim 1, wherein the speeding logic circuit is arranged to control the counting rate of the counter circuit, and thus the display driver current, based on the output of the speeding comparator so as to converge the display driver current to said predetermined value.

3. (Previously Presented) The RGB control circuit of claim 2, wherein said speeding logic circuit produces a RGB output blanking signal whilst said display driver current is substantially different from said predetermined value.

4. (Previously Presented) The RGB control circuit of claim 3, including control circuits for each of the colour channels, and wherein said speeding logic circuit produces said RGB

output blanking signal based on the counting rate of any and/or each of the counter circuits for the colour channels.

5. (Previously Presented) The RGB control circuit of claim 1, wherein the speeding comparator 30 has a plurality of outputs including a convergent output and at least one upper output and lower output, and wherein said convergent output corresponds to said display driver current being substantially equal to said predetermined value and said upper and lower outputs are utilised by said speeding logic circuit to determine the up/down counting rate of the counter circuit.

6. (Previously Presented) The RGB control circuit of claim 5, wherein each of said upper and lower outputs correspond to respective up and down binary counting rates for said counter circuit.

7. (Previously Presented) The RGB control circuit of claim 1, wherein the counter circuit and the analog output circuit are both 9-bit circuits.

8. (Previously Presented) The RGB control circuit of claim 1, further comprising a current reference circuit comprising a comparator coupled to the display driver current sensor and to a capacitor.

9. (Previously Presented) The RGB control circuit of claim 1, further comprising a warm-up circuit comprising a comparator having a first input coupled to the display driver current sensor and a second input coupled to a starting voltage source.

10. (Currently Amended) An RGB control circuit for use in television and video display control, comprising:

an up/down counter circuit configured to receive a display driver current and to generate a digital output signal in response thereto;

a digital-to-analog converter having an input coupled to an output of the counter circuit and configured to receive the digital output signal from the counter circuit and to output an analog control signal;

a speeding comparator circuit comprising a plurality of comparators, each comparator having an input coupled in parallel with the other comparator circuits to a cathode current output for determining and outputting a measure of a difference between the cathode current output and a predetermined value; and

a speeding logic circuit having an input coupled to an output of the speeding comparator circuit and further having a first output coupled to the counter circuit, the speeding logic circuit configured to control the counting rate of the counter circuit according to a measure of a difference between the cathode current and the predetermined value to provide a variable up counting rate and a variable down counting rate.

11. (Previously Presented) The circuit of claim 10, wherein the speeding logic circuit comprises a second output on which is generated an RGB output blanking signal to blank the RGB output when the control circuit is unstable as determined by the output of the speeding comparator.

12. (Previously Presented) The circuit of claim 10, wherein the speeding logic circuit is configured to control a counting rate of the counter circuit based on the output of the speeding comparator in order to converge the cathode current to the predetermined value.

13. (Previously Presented) The circuit of claim 10, wherein the counter circuit comprises a 9-bit up/down counter, and further wherein the digital-to-analog converter comprises a 9-bit digital-to-analog converter.

14. (Previously Presented) A digital cut-off control loop circuit for television and video display control, comprising:

a display driver current sensor;

an up/down counter circuit having an input coupled to the display driver current sensor and an output;

an analog output circuit having an input coupled to the output of the up/down counter and an output coupled to control the display driver current;

a speeding comparator comprising a plurality of comparator circuits each having an input coupled in parallel with the display driver current sensor and configured to determine and output a measure of the difference between a sensed display driver current and a predetermined value;

a speeding logic circuit having an input coupled to an output of the speeding comparator and having an output coupled to a further input of the up/down counter circuit for controlling a counting rate of the up/down counter circuit according to a measure of a difference between the display driver current and the predetermined value;

a current reference circuit comprising a comparator having a first input coupled to the display driver current sensor and a second input coupled to a leak voltage reference source and an output coupled to a capacitor; and

a warm-up circuit comprising a comparator having a first input coupled to the display driver current sensor and a second input coupled to a starting voltage source.

15. (Previously Presented) The circuit of claim 14, wherein the speeding logic circuit is configured to generate a control signal while the display driver current is substantially different from the predetermined value.

16. (Previously Presented) The circuit of claim 14, wherein the speeding comparator comprises a plurality of outputs including a convergent output and at least one upper output and lower output, and wherein the convergent output corresponds to the display driver current being substantially equal to the predetermined value, and the upper and lower outputs are utilised by the speeding logic circuit to determine the up/down counting rate of the counter circuit, respectively.

17. (New) An RGB control circuit for use in television/video display control, comprising:

a display driver current sensor;

a 9-bit counter circuit and 9-bit analog output circuit coupled to control the display driver current;

a speeding comparator having a plurality of comparator circuits coupled in parallel with the display driver current sensor as input, for determining and outputting a measure of the difference between the sensed display driver current and a predetermined value thereof; and

a speeding logic circuit coupled to the speeding comparator and counter circuit, and arranged to control the up/down counting rate of the counter circuit according to said measure of difference in display driver current, wherein the counter circuit and the analog output circuit are both 9-bit circuits.

18. (New) An RGB control circuit for use in television and video display control, comprising:

an up/down 9-bit counter circuit configured to receive a display driver current and to generate a digital output signal in response thereto;

a 9-bit digital-to-analog converter having an input coupled to an output of the counter circuit and configured to receive the digital output signal from the counter circuit and to output an analog control signal;

a speeding comparator circuit comprising a plurality of comparators, each comparator having an input coupled in parallel with the other comparator circuits to a cathode current output for determining and outputting a measure of a difference between the cathode current output and a predetermined value; and

a speeding logic circuit having an input coupled to an output of the speeding comparator circuit and further having a first output coupled to the counter circuit, the speeding logic circuit configured to control the counting rate of the counter circuit according to a measure of a difference between the cathode current and the predetermined value to provide a variable up counting rate and a variable down counting rate, wherein the counter circuit comprises a 9-bit up/down counter, and further wherein the digital-to-analog converter comprises a 9-bit digital-to-analog converter.